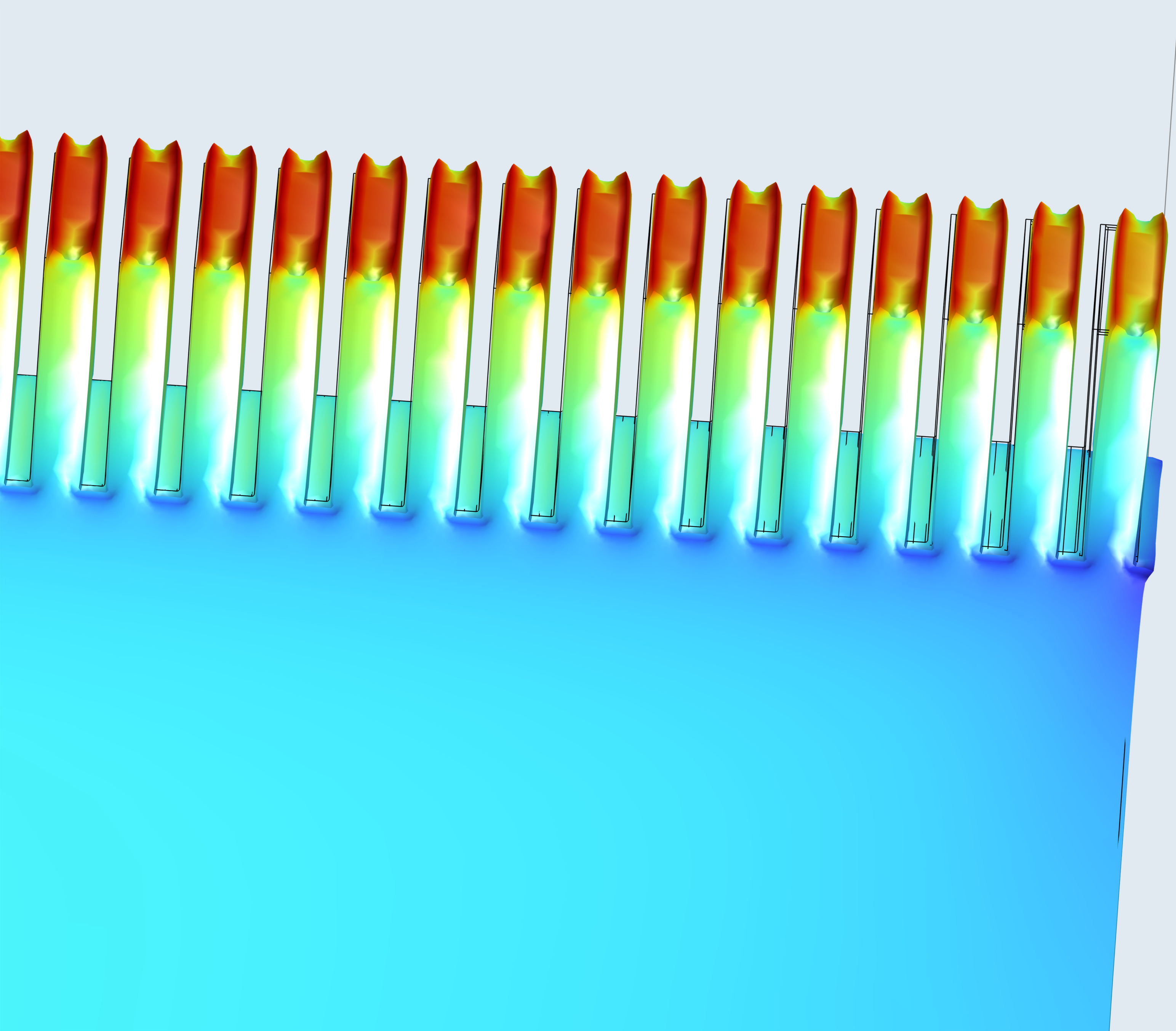

Predictive Simulations of Warpage Phenomena on Arbitrarily Patterned Silicon Wafers

Warpage is one of the most important challenges in microelectronics after the advent of 300-mm wafers. Preventing and understanding this phenomenon would provide great benefits in terms of time saving and monetary costs.

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Introduction

One of the major challenges that has emerged from the transition to 300 mm is the increase in warpage phenomena. Without predictive methods, the only way to limit this issue has been through trial and error, looking for less warpage upon changing geometries and materials in use. This process is obviously slow and expensive as it requires continuous rewriting of the design and costly waste of material.

In my PhD project, in collaboration between Politecnico di Milano and ST Microelectronics, COMSOL® simulations will be used to better comprehend and limit the warpage phenomena in a IGBT power device.

This system presents a highly directional patterning, with thousands of trenches aligned along the vertical direction. This geometry leads to critical warps with asymmetric saddle shapes most probably given by the strong dimensional ratio between width (~1 µm) and length (~1 mm) of each trench.

In order to study the system with COMSOL Multiphysics®, a general approach has been developed passing from a unitary cell to the complete wafer. While still in its early stages this project could lay the foundation for a predictive analysis system to prevent the warpage problem, initially designed for the IGBT but potentially transferable to a wide range of other devices.

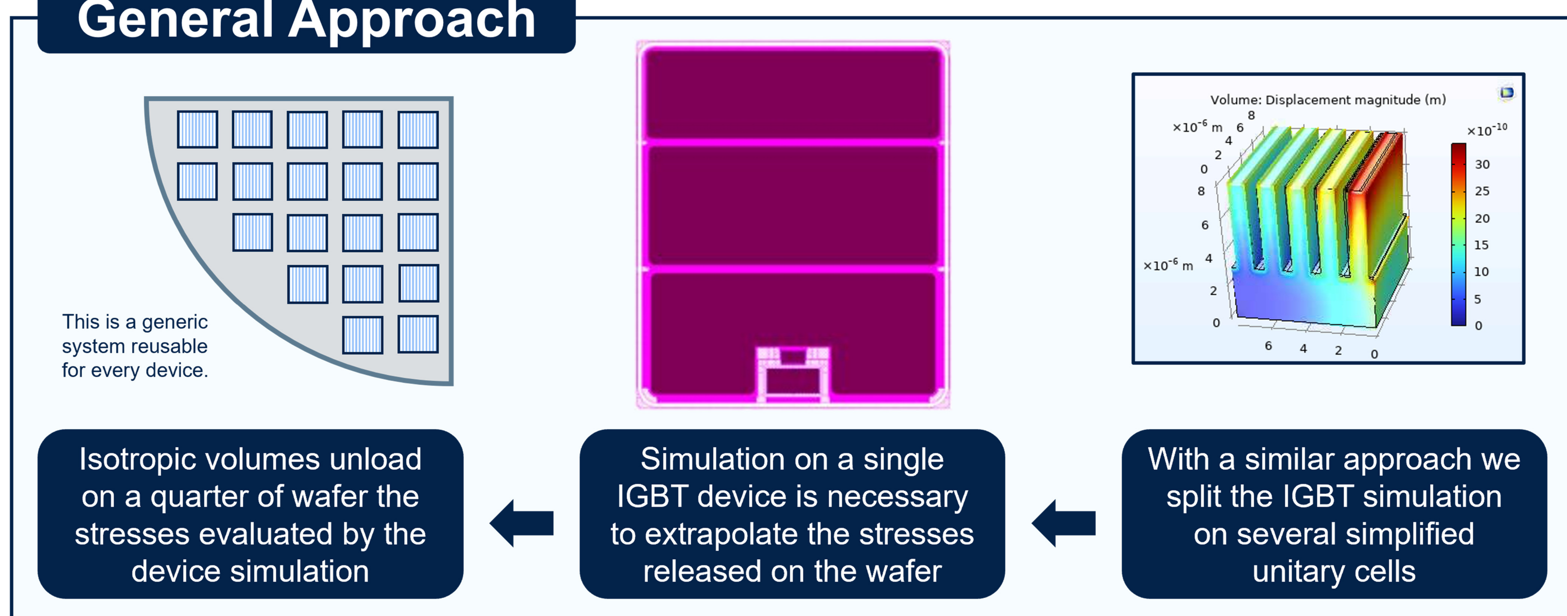

FIGURE 1. The approach consist in three phases, going from the simulation of a unitary cell, to that of the complete device, ending with the transposition to a quarter of wafer. The specific device geometry is not considered anymore in the last step.

Methodology

The objective of the Project is to obtain a graphical representation of the deformed wafer by exploiting the intrinsic stresses of the materials involved, measured during the process steps that are to be simulated. Through the stress, which can be evaluated by a series of characterizations on flat wafers, it is possible to directly obtain the deformation without considering thermal budgets or steps that lead to geometry modification. Simulating in a single stage the entire wafer would still require an unattainable computational power, so it will be necessary to divide the simulation into 3 main steps:

- Consider a quarter wafer in which individual devices are replaced by isotropic, non-patterned volumes that unload specific stresses on the structure.
- These stresses will be the result of a simulation of the individual device (the geometry of the specific product comes into play).
- To simulate the device, it is necessary to work on a unitary cell that can reduce the computational load.

Results

The Project is still in its early stages and under development. Initial work has been devoted to the production and characterization of flat wafers, necessary to extrapolate the intrinsic stresses of the materials involved in the three process steps to be simulated (gate oxide deposition; poly-filling of the trenches; high temperature thermal treatment, called Body Annealing). Through Stoney's equation (1), it was possible to derive the stress of each material involved from the wafer profiles.

$$\sigma_i = \frac{1}{6}\frac{E_{Si}}{1-\nu Si}\frac{(\sum_1^i t_i - 1)^2}{t_i}\left(\frac{1}{R_i} - \frac{1}{R_i - 1}\right) \quad (1)$$

The same process was repeated following the Body Annealing, since the intrinsic stress depends on the thermal budget seen by the material. However, this value does not depend on the geometry of the device, so with the same deposition process, the calculated stress will be valid for any future simulation.
With the stresses evaluated and tested through flat wafer "retest" simulations, it is possible to continue the Project with the first unit cell simulation.

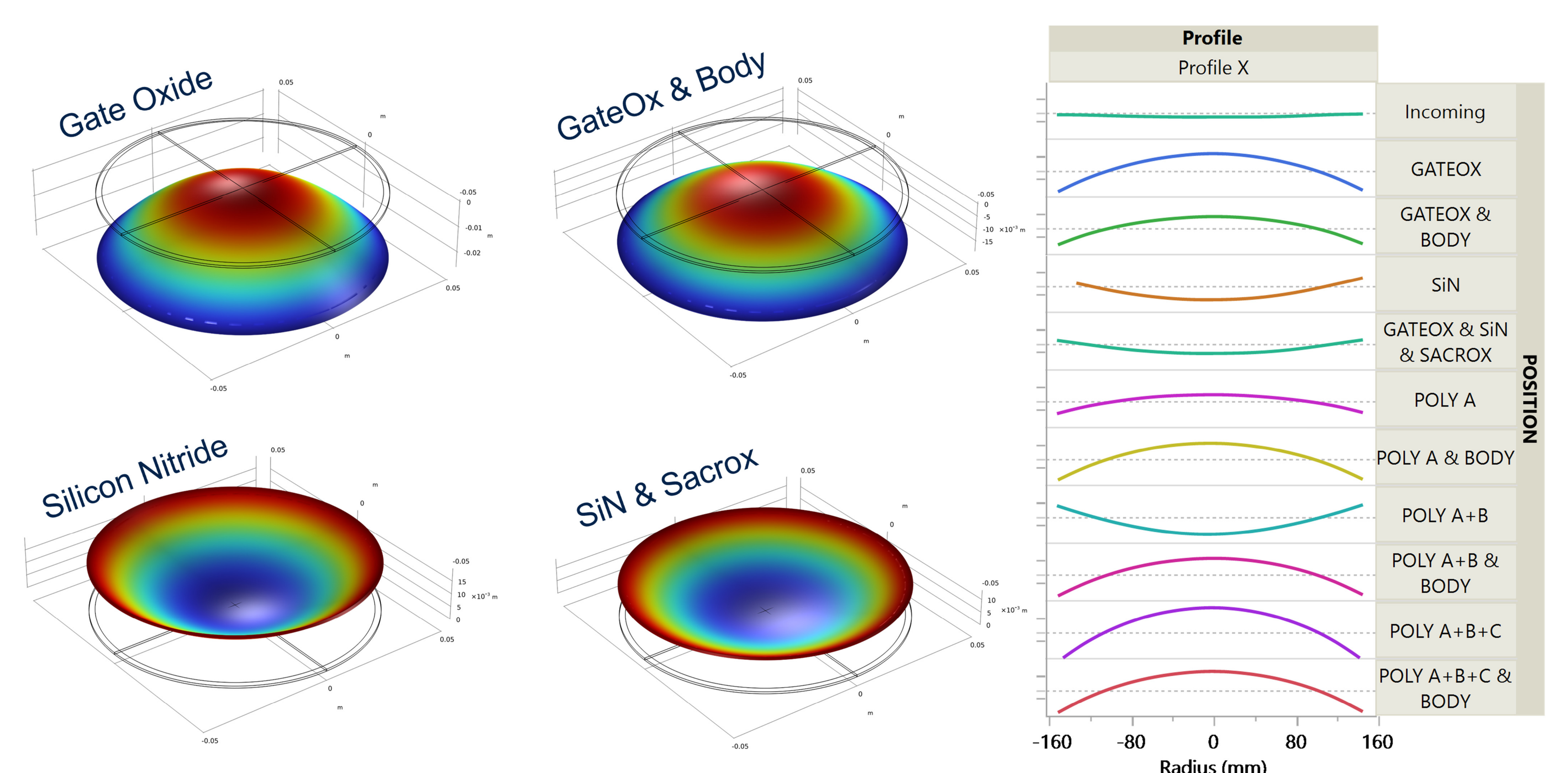

FIGURE 2: Simulation results of the warped flat wafers after gate oxide deposition (GateOx) and Nitride deposition before and after thermal treatment (*on the left*) and wafer warped profiles in each of the process steps involved in the simulation (*on the right*).

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