Electron Beam Crystallization of Amorphous Silicon Thin Films

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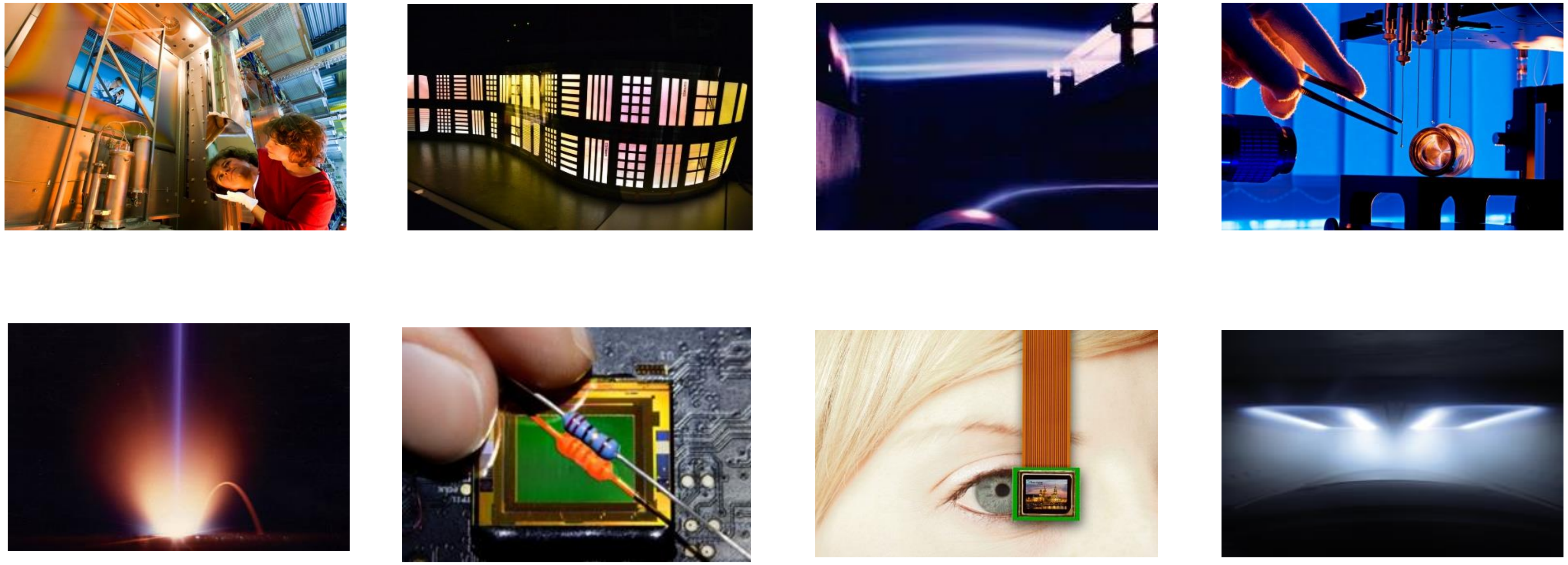

Outline

- Motivation
- Methods and numerical model
- Results and Discussion
- Conclusion and Outlook

Motivation


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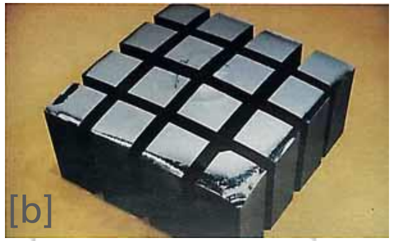
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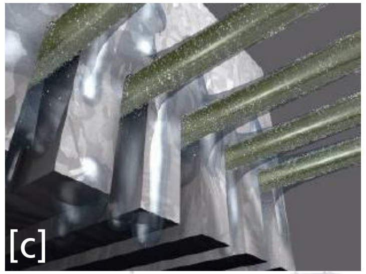
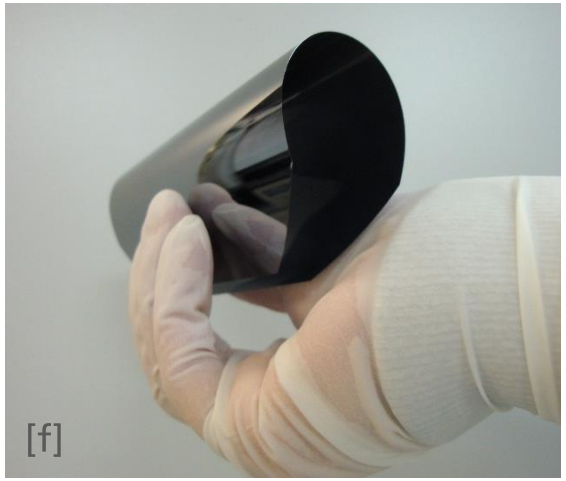

[c]


[d]


[e]

kerfloss ~ 30-50% high purity silicon (10^8 kg/year) [1,2]
= huge saving potential for manufacturing costs


[f]

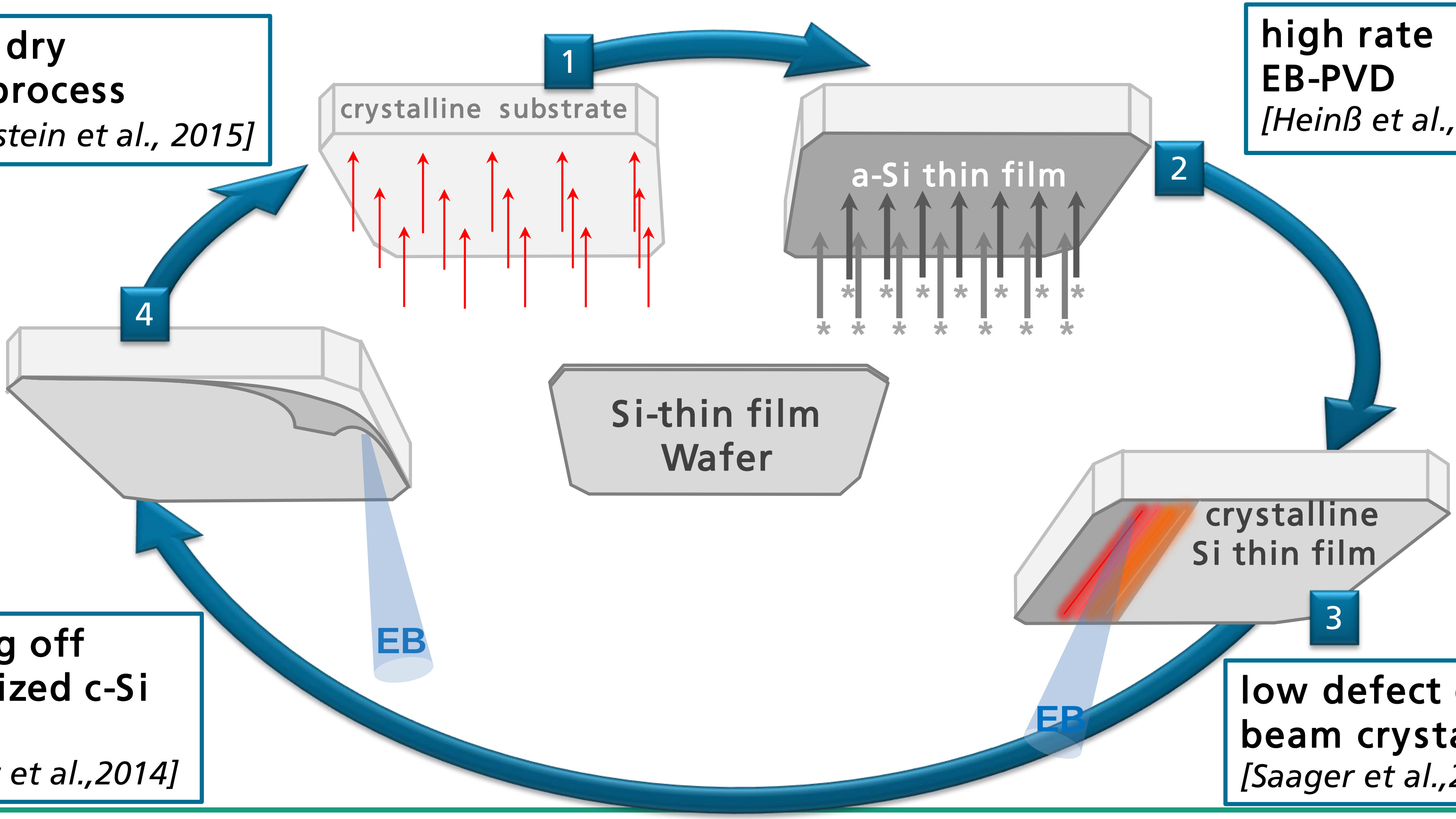
kerfless = no material waste + very thin wafers
= long-term future technology

[1] P. Keller et al., *in Proceedings of EU PVSEC*, Amsterdam, pp. 603-607, 2014
[2] A. Jäger-Waldau, JRC's 2014 PV Status Report,, Report EUR 26990 EN

[Metzner et al., 2015]

Motivation

- kerfless wafering Technologie am *Fraunhofer FEP* -



**_in situ_ dry
clean process**
[Bodenstein et al., 2015]

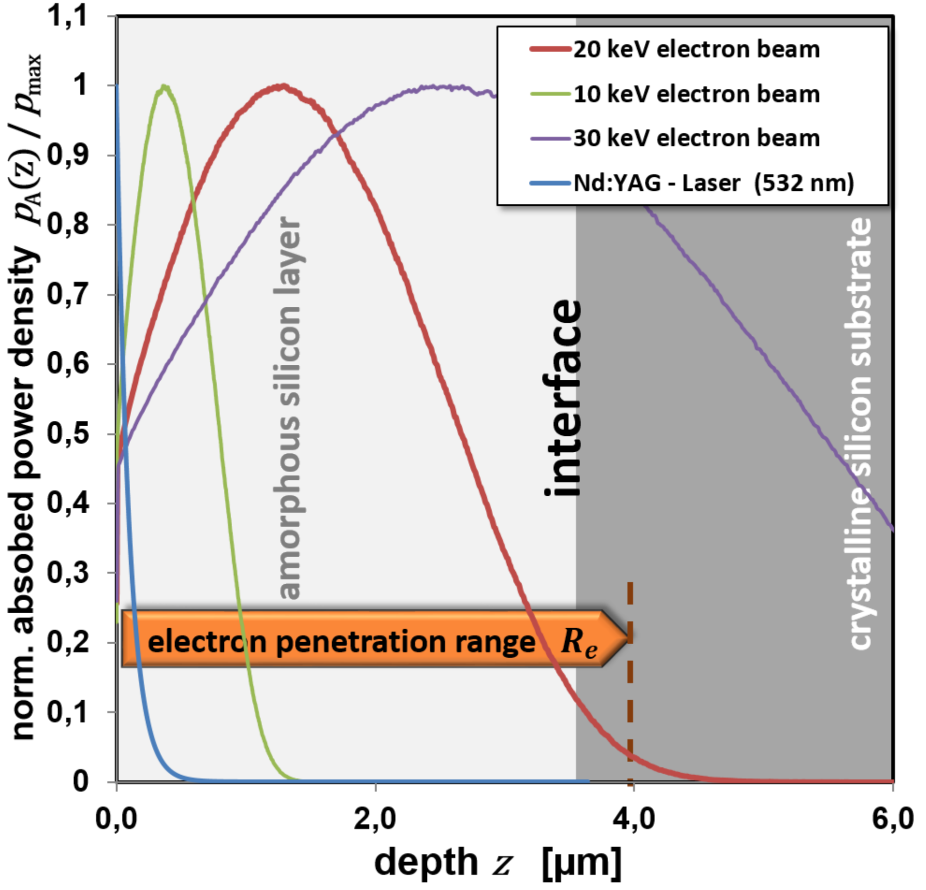
**high rate
EB-PVD**
[Heinß et al., 2015]

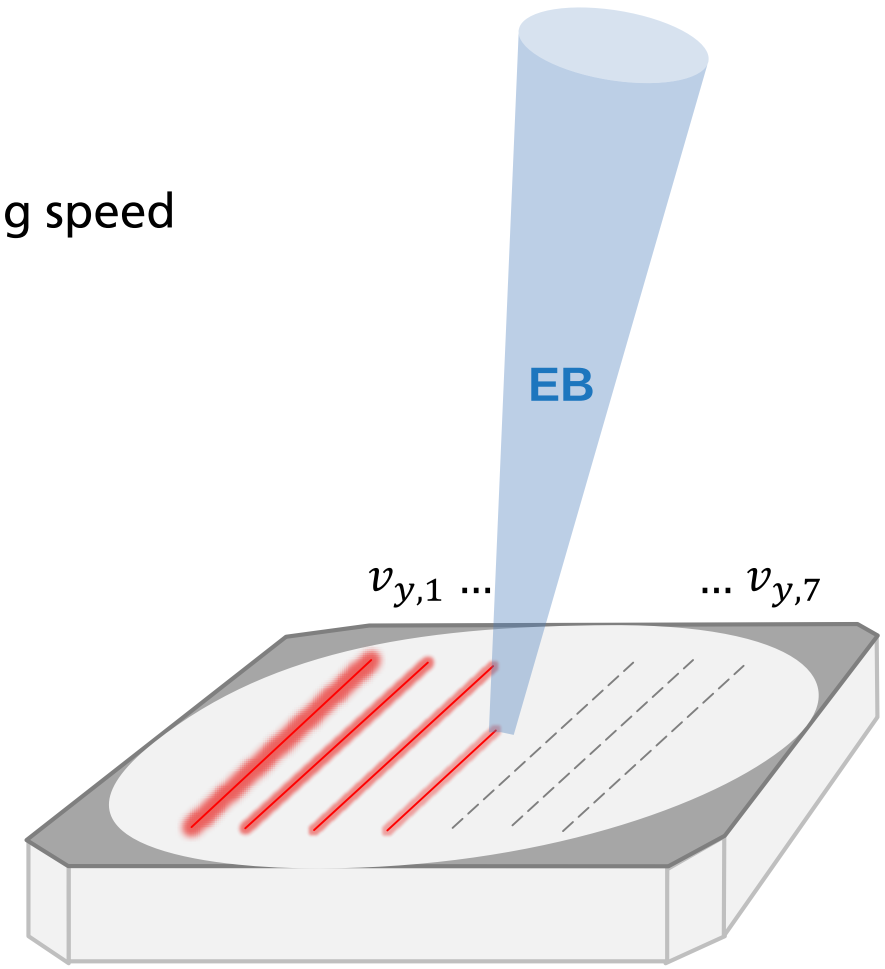
**low defect electron
beam crystallization**
[Saager et al.,2014]

**splitting off
crystallized c-Si
layer**
[Temmler et al.,2014]

Methods and Numerical Model

- using a-Si coated Si-Wafers
- electron beam line scribing with different line scanning speed





Methods and Numerical Model

- For temperature field - solving 3D heat equation

$$c_p(T)\rho(T)\frac{\partial T(\vec{r},t)}{\partial t} - \nabla[\lambda(T)\cdot\nabla T(\vec{r},t)]$$

$$= p_A(\vec{r},t) - \rho(T)\frac{\partial h_{\text{fus}}}{\partial t}$$

$$\boxed{e_A(x,y) = \frac{1}{R_e}\iint p_A(\vec{r},t)\,\mathrm{dt}\,\mathrm{dz}}$$

$$p_A(\vec{r},t) = \eta_{th}U_B\cdot j_B(x,y,t)\frac{f_A(z)}{R_e}$$

$$T(\vec{r},t=0) = T_{ini} \qquad \forall\vec{r}\in\mathcal{K}$$

$$-\lambda(T)\cdot\vec{n}\cdot\nabla T(\vec{r},t) = \varepsilon(T)\cdot\sigma_{SB}(T_U^4 - T^4), \qquad \forall\vec{r}\in\partial\mathcal{K}$$

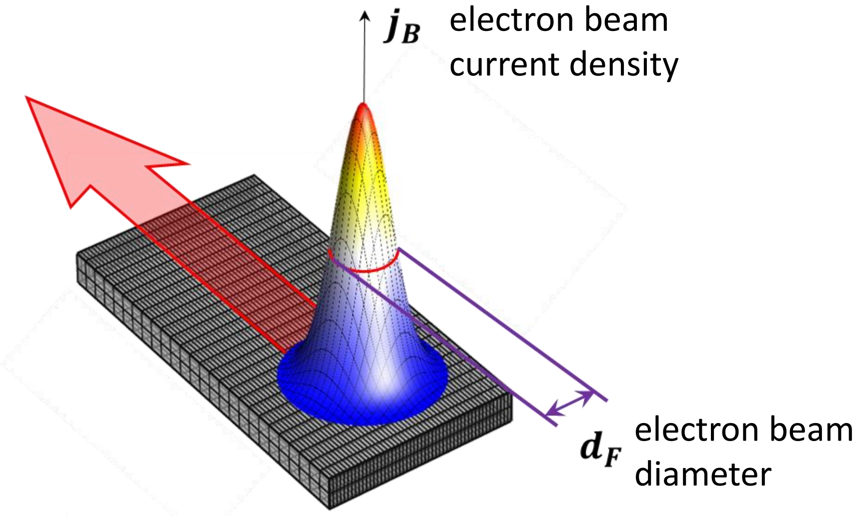
- For stress field – considering thermal and initial stress

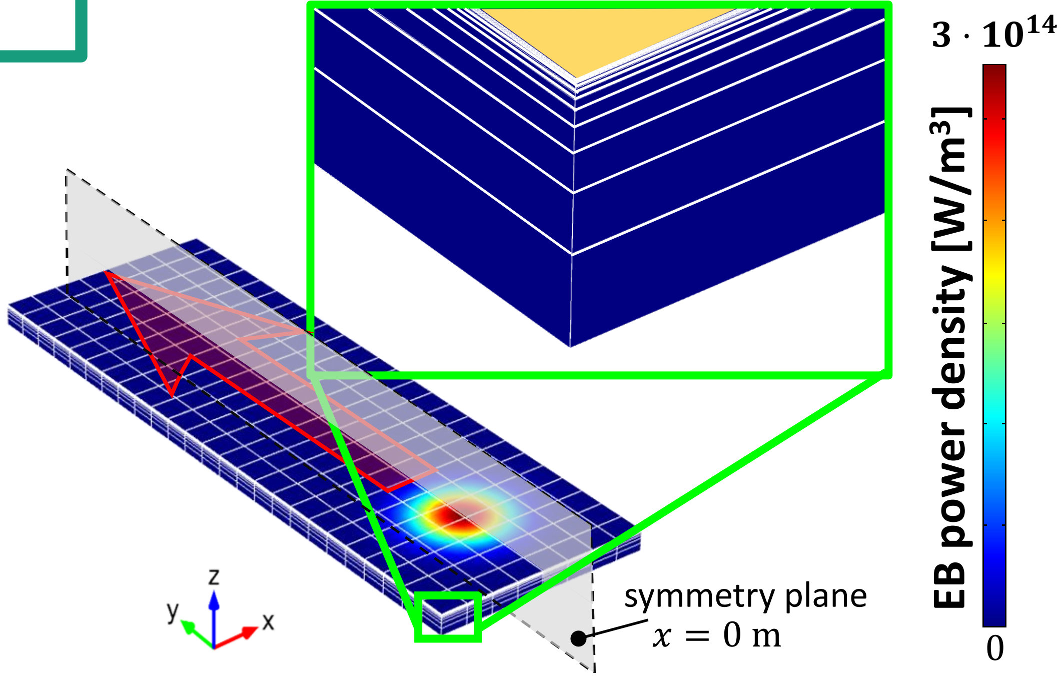
$$\hat{\sigma} = \hat{\sigma}_{ini} + \hat{C}:\hat{\epsilon}^{\sigma}$$

$$\boxed{w_\sigma = \frac{1}{2}\cdot\int_0^d \hat{\sigma}:\hat{\epsilon}^{\sigma}\,\mathrm{dz}}$$

$$\hat{\epsilon}^{\sigma} = \hat{\epsilon} - \hat{\epsilon}_0 - \hat{\epsilon}^{\text{th}}$$

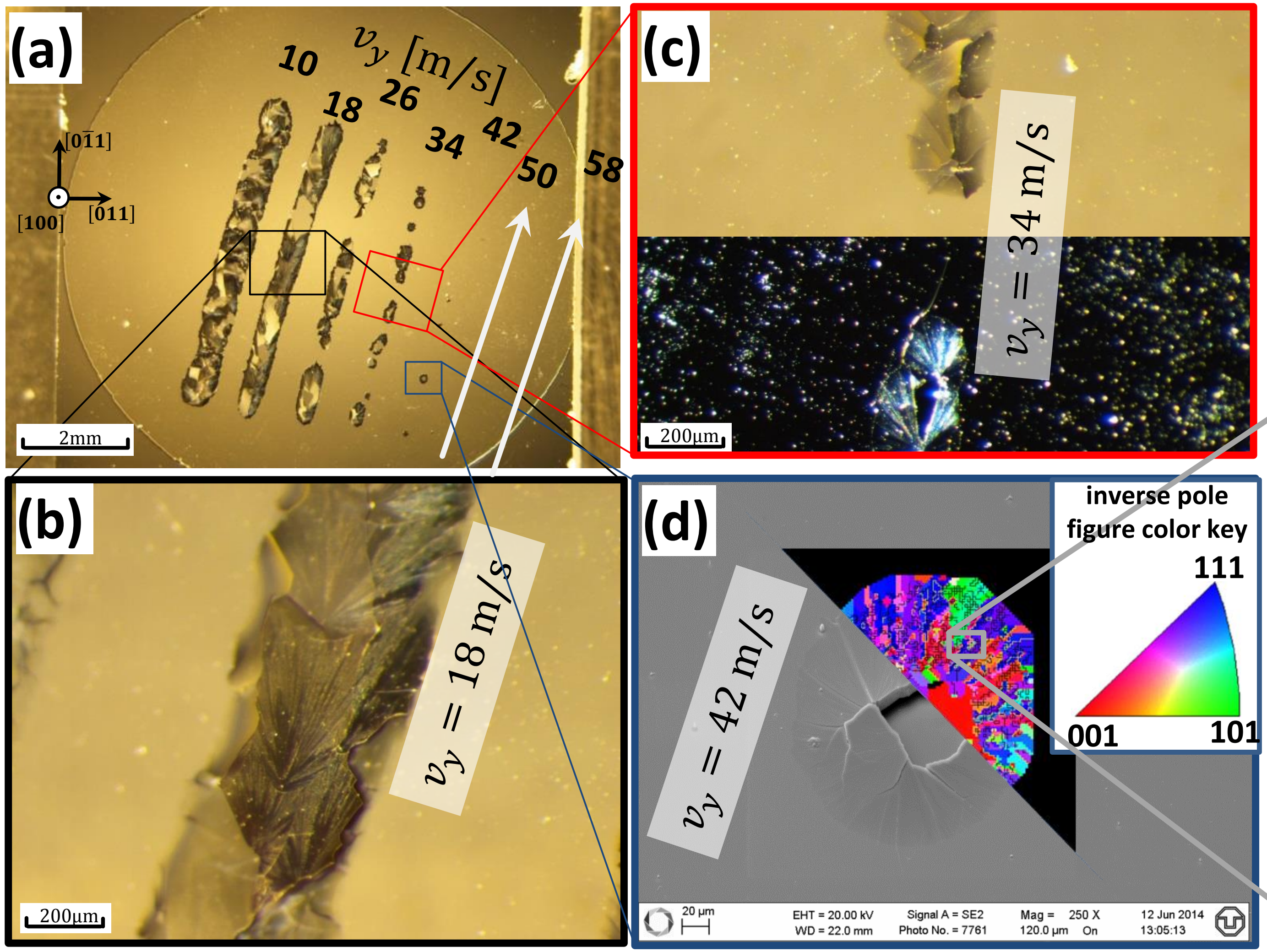
$$\hat{\epsilon}^{\text{th}} = \hat{\alpha}(T)\cdot(T(\vec{r}) - T_{\text{ref}})$$



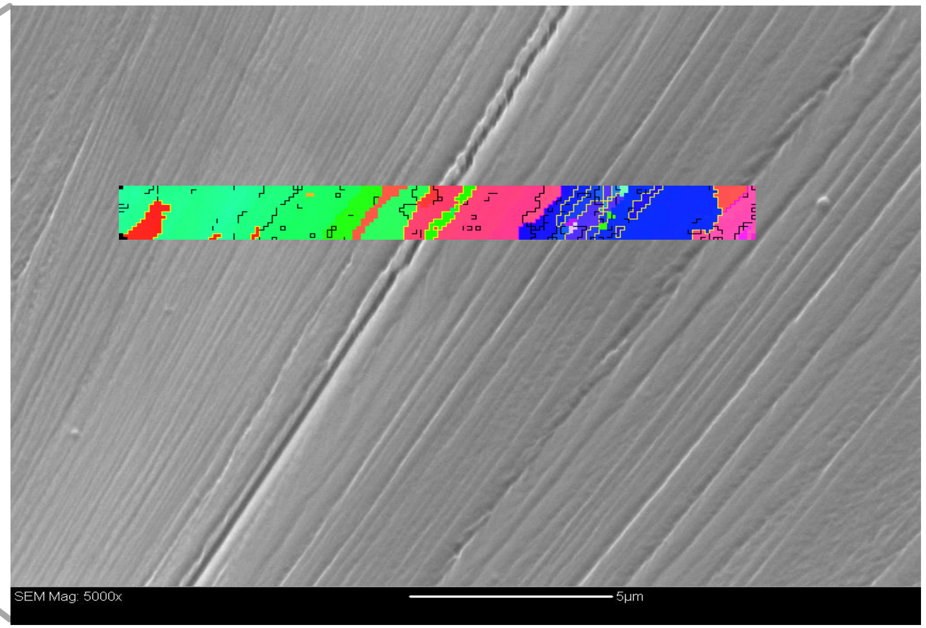


Experimental Results

- line scribing on a-Si coated Si-Wafer by electron beam-

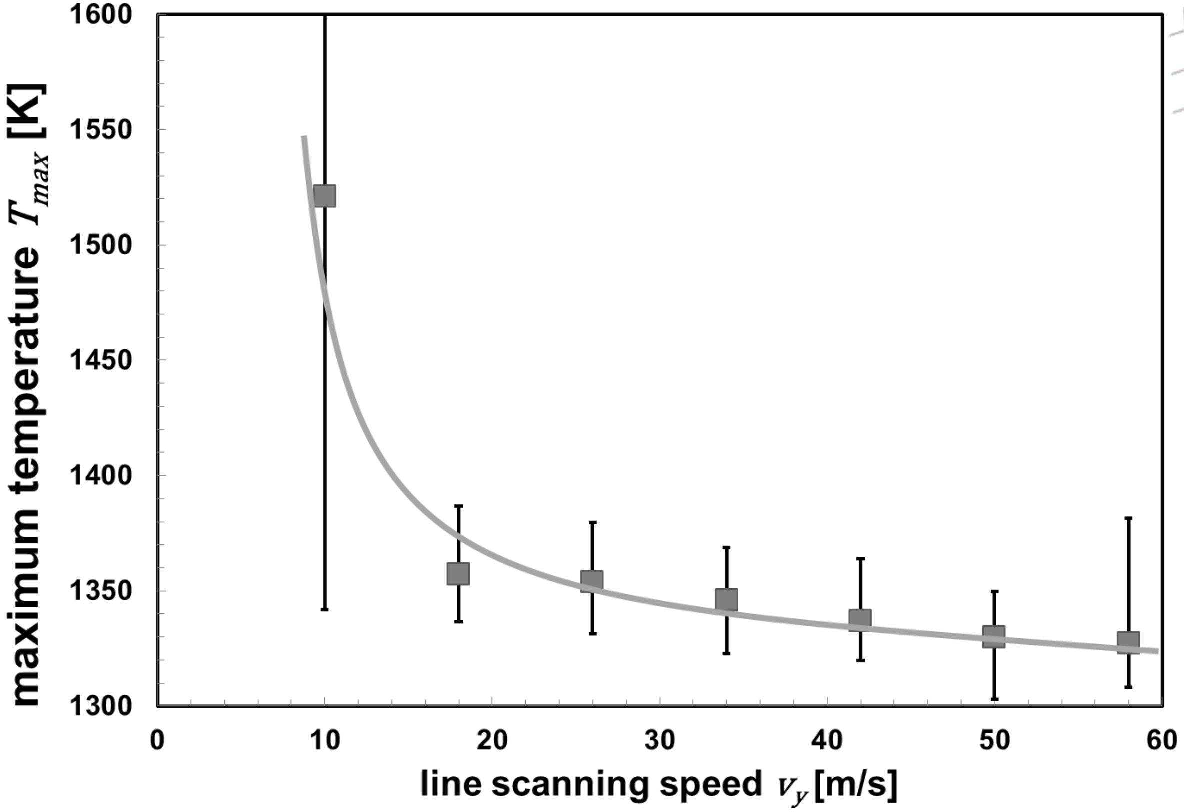


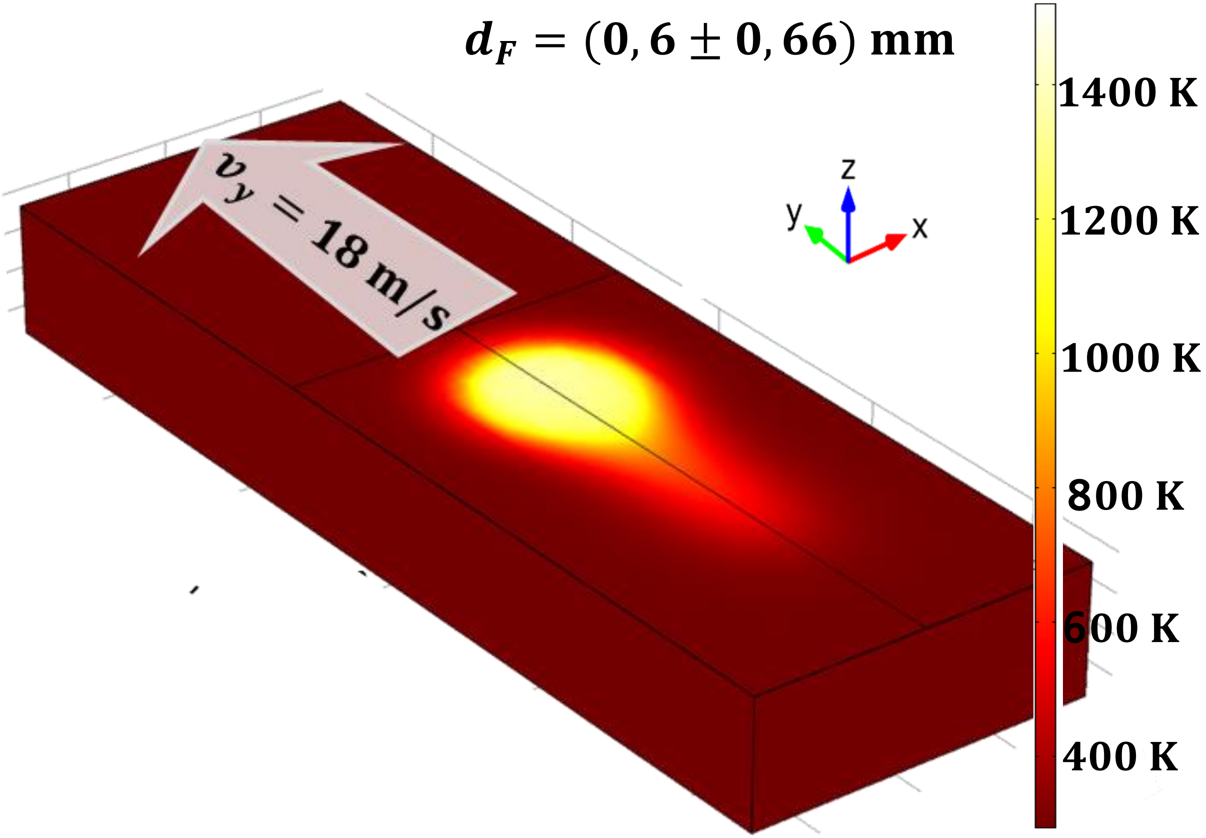
- layer delamination at certain areas for $v_y \geq 50\,\mathrm{m/s}$ and $e_A \leq 7\,\mathrm{kJ/cm^3}$, resp.
- still attached layer regions are still amorphous
- detached layer regions shows a fine grained structure with long crystallites and with random crystal orientation
  ➔ explosive solid phase crystallization



Numerical Results

- simulation of the temperature field -



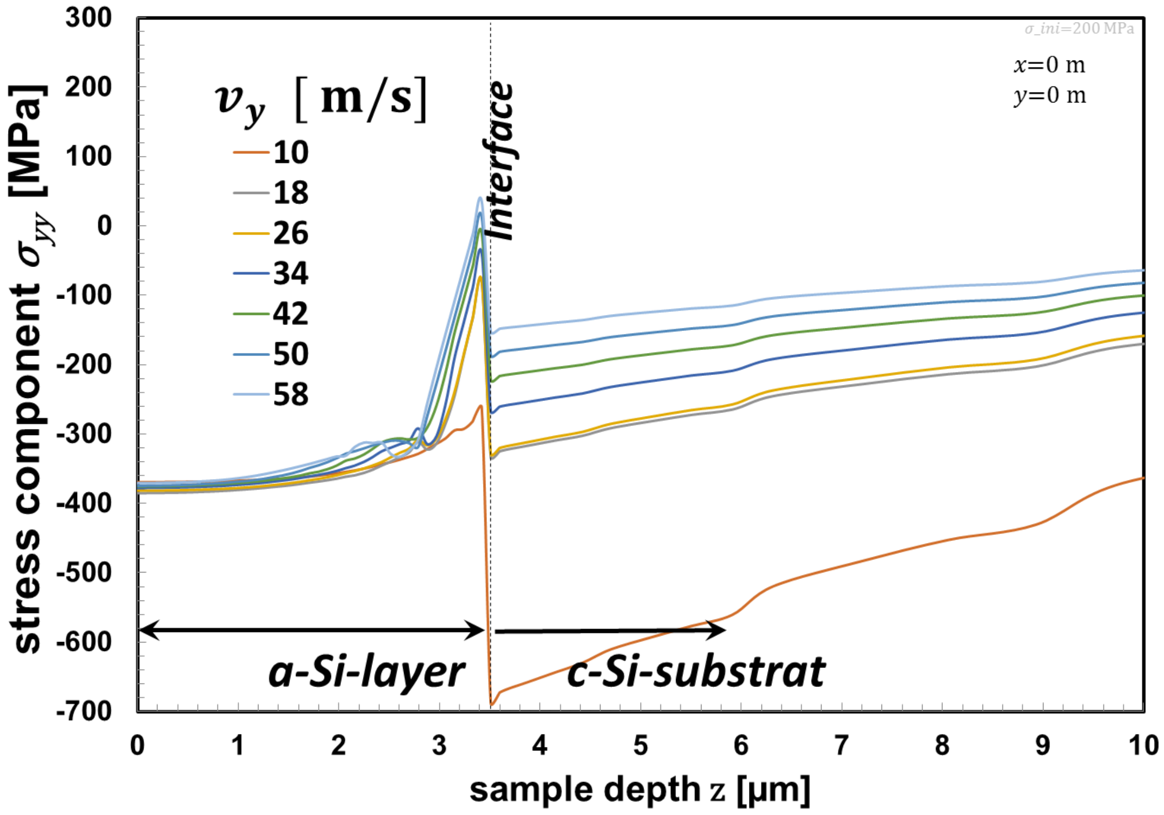


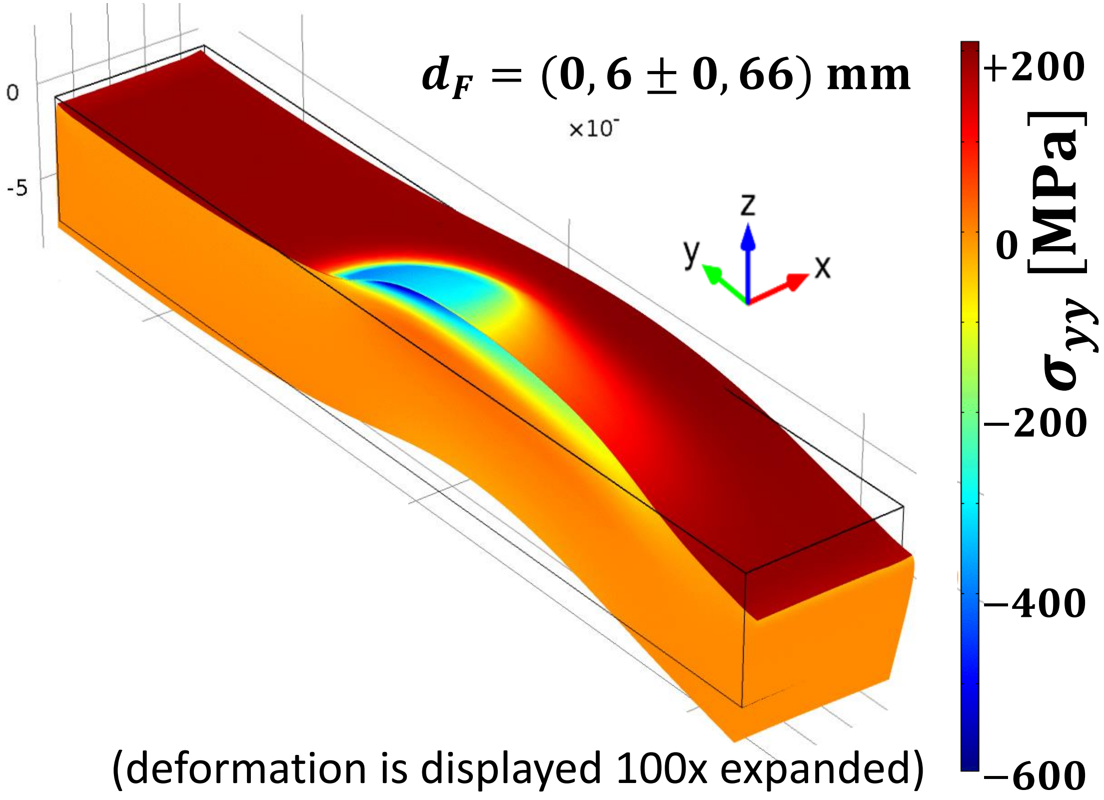
- $T_{\max} < T_{a-l} \approx 1420$ K (crystallization temperature)

➔ No crystallization phenomena would be expected

Numerical Results

- simulation of the thermal stress field -





(deformation is displayed 100x expanded)

- Initial tensile layer stress σ_{ini} will be compensated by compressive thermal stress
- maximum stress value of the σ_{yy}-component shows little variation in the a-Si layer

➔ Delamination phenomena can not be explained

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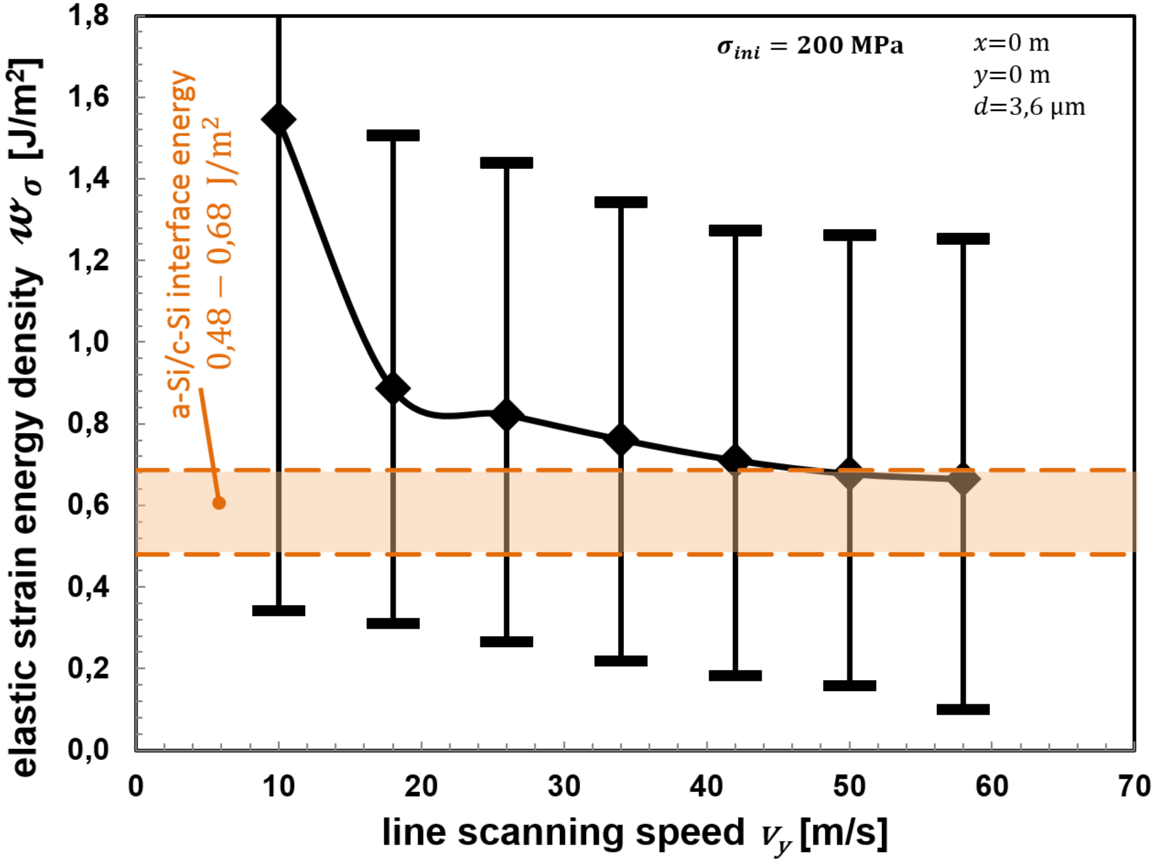
Numerical Results

- simulation of the thermal stress field -

➔ energetic consideration of stress conditions -



areal elastic strain energy density

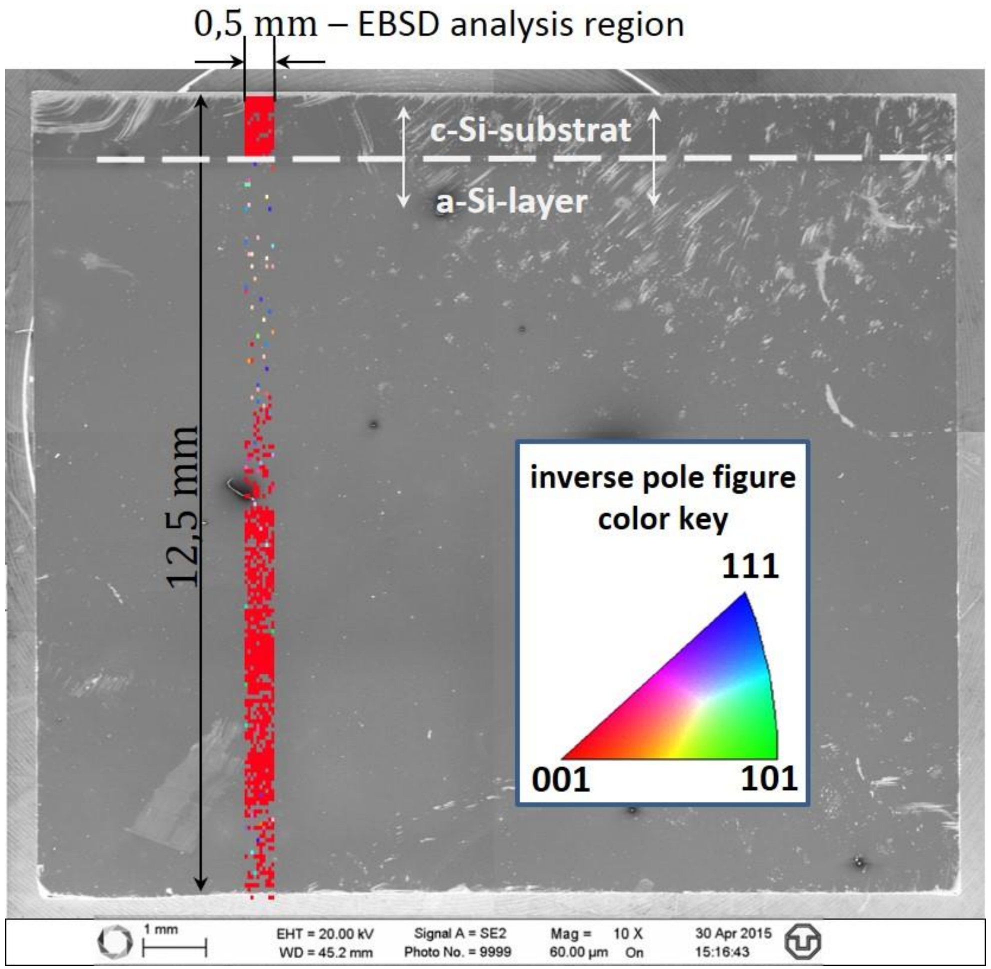
$$w_\sigma = \frac{1}{2} \cdot \int_0^d \hat{\sigma} : \hat{\epsilon}^\sigma \, dz$$

- Rising elastic strain energy desisty w_σ with increasing absorbed electron beam energy e_A
- Layer delamination will be expected if the stored mechanical energy exceeds the interface energy.
  This is the case for
  $v_y \geq 50\,\mathrm{m/s}$ and $e_A \leq 7\,\mathrm{kJ/cm^3}$, respectively

➔ plausibel reason for layer delamination phenomena

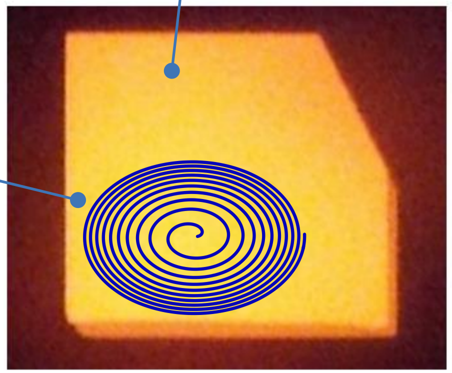
Experimental Results

- additional crystallization tests with *extended scanning* pattern -



- Slowly heating up the whole sample to the maximum of $T_{\max} \approx 1500\ \mathrm{K}$
- No layer delamination observed !
- layer crystalizes with the same (001) crystal orientation from Si-substrate

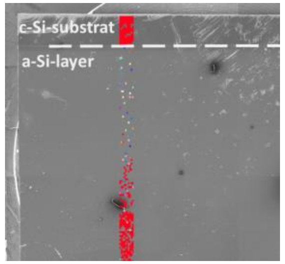
➔ <u>epitaxial solid phase crystallization</u>

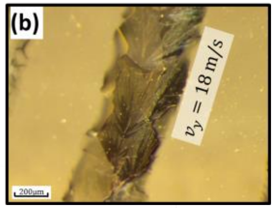


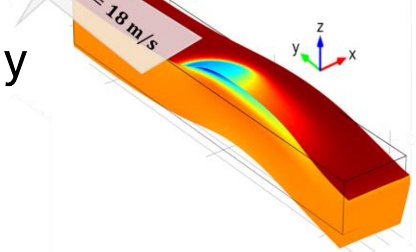
glowing sample during electron beam processing

applied scanning pattern with high repletion rate at lower EB power line pitch $\ll d_F$

Conclusion and Outlook







- electron beam treatment on a-Si coated Si-substrates
  - ➢ epitaxial regrowth to (001) crystal orientation from Si-substrate
  - ➢ Increasing EB power density for enhancing throughput ➔ layer delamination
    Reason???
- COMSOL® simulation ➔ accumulation of strain energy up to interface energy
  ➔ simulation results agree very well with experiment
- with FEM simulations ➔ an efficient process optimization is possible
  ➔ undetectable process states can be find out
  ➔ unexplainable processes phenomena can be understood
- Further working tasks ➔ further process optimization
  ➔ determine process limits for enhancing throughput

Fraunhofer FEP mission ➔ enhancing of competences for the simulation of thermal and mechanical processes
➔ looking for project partners for extending further systematical studies

Thank you very much for your attention !

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Image References

(19.11.2015)

[a] http://www.silfex.com/products_2_0.html
[b] http://www.udo-leuschner.de/basiswissen/SB110-05.htm
[c] http://www.pv-tech.org/news/tool_order_meyer_burger_receives_first_technology_buy_contracts_in_2_years
[d] http://www.wirautomatisierer.de/image/image_gallery?img_id=34993854
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