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CdS Thin Film Transistor Threshold voltage shift investigation

Wudyalew Wondmagegn

Department of Physics and Engineering, Frostburg State University, Frostburg MD 21532, USA, *Phone: (301)687-7072, Fax: (301)687-7966, E-mail: wwondmagegn@frostburg.edu*

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Content

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  - Inverter
  - OPAMP
- Device Simulation Approaches
  - Uniform distribution of traps
  - Multigrain structure
- Results
- Conclusion

Circuit applications tested with CdS transistor

Inverter

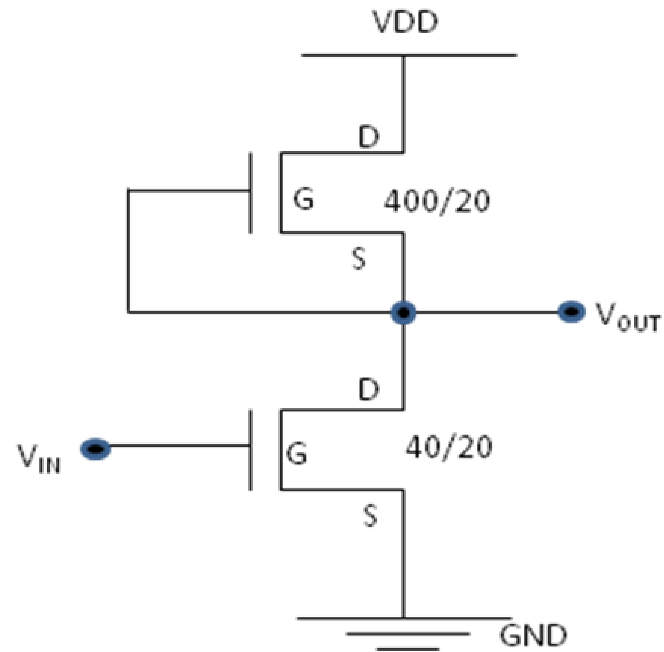
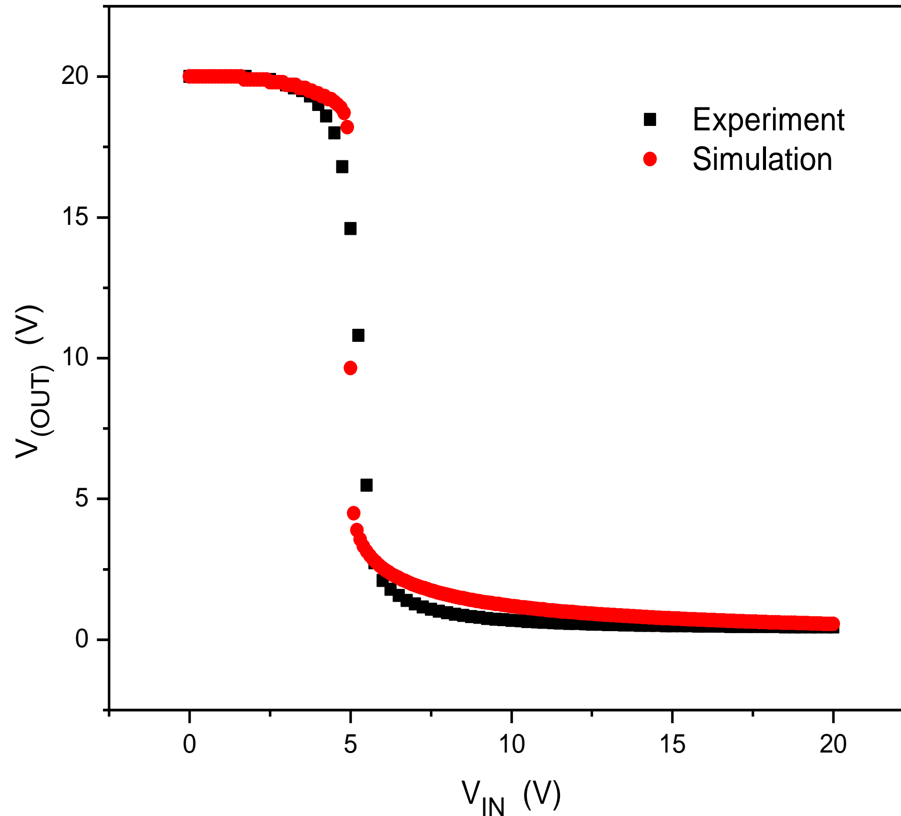


Fig.1 Inverter schematic based on CdS TFT

- Active load inverter
- Transistors are defined as a physical device.

Transfer curve



- Uniform trap distribution employed
- The simulation suggested a slight difference interface charge between the load and switching transistor
- Best match with $3x10^{11}$ cm^{-2} and 10^{12} cm^{-2} interface charges for the switching and load transistors respectively.
- Results threshold voltage difference

Fig.2 Simulation Input-Output characteristics of the inverter.

Operational Amplifier

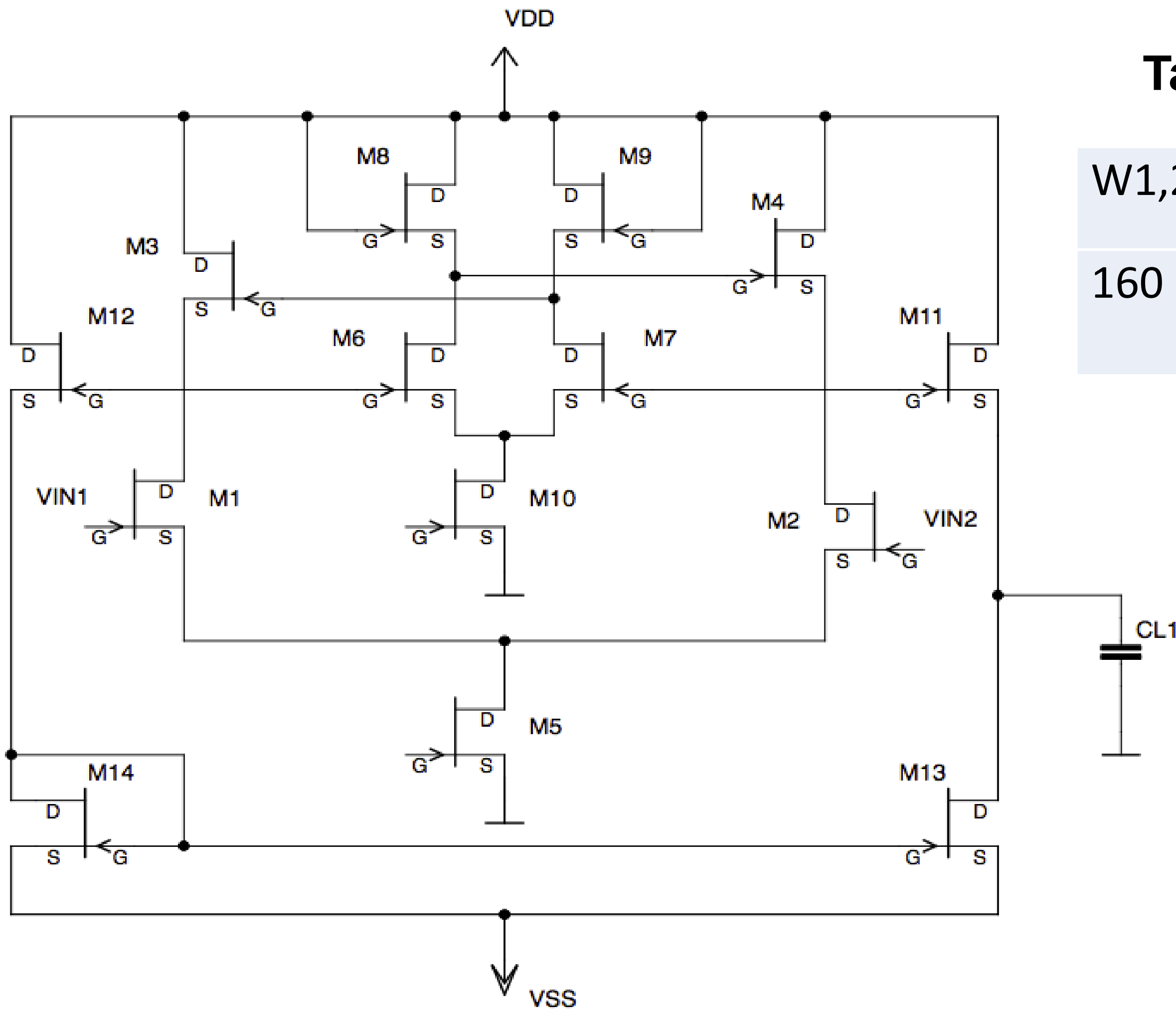


Fig.3 Circuit schematics of all n-type topology

Table 1. Design parameters

W1,2,6,7	W3,4	W5	W11-14	W8,9	W10	L
160 μm	100 μm	280 μm	320 μm	120 μm	320 μm	20 μm

CL	VDD,VG_M10, VG_M5	VSS
10p	20 V	-20 V

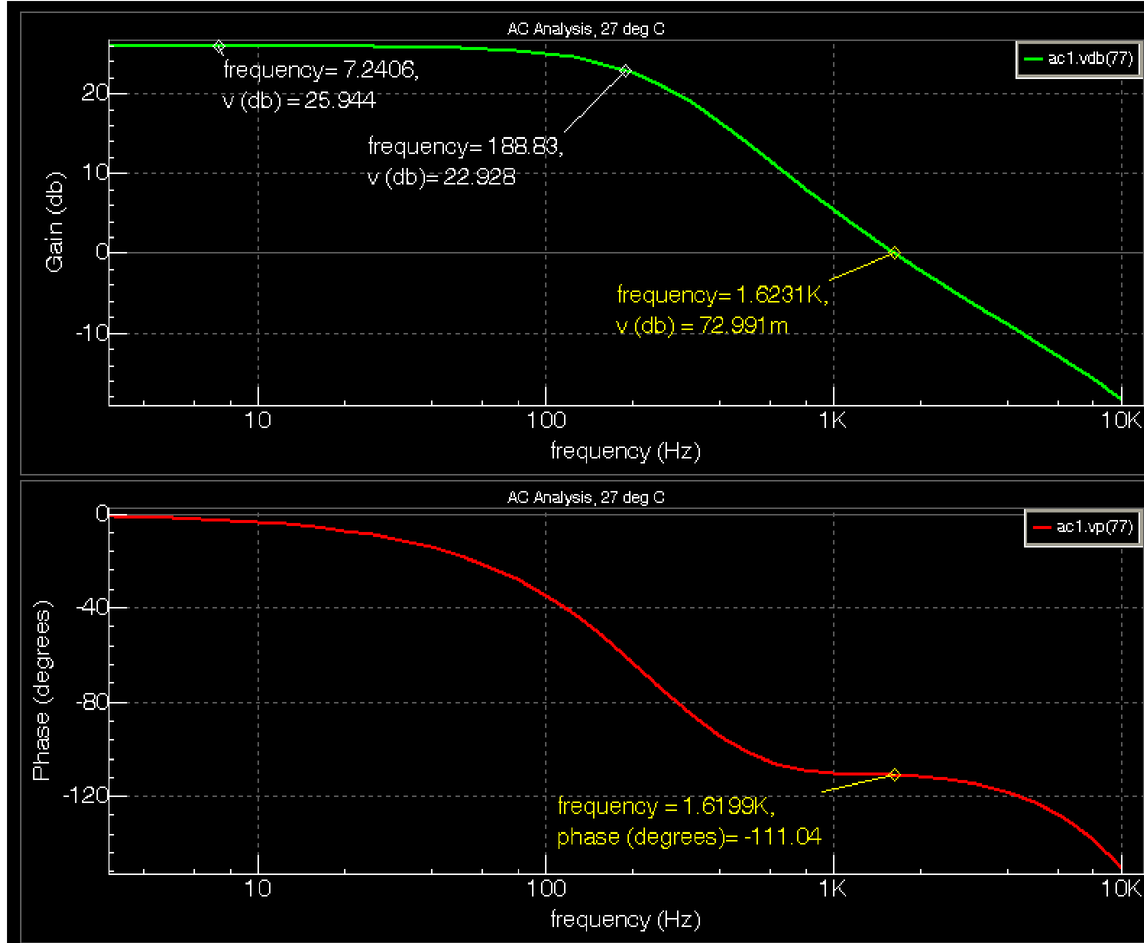


Fig.4 Gain and Phase plots

Table 2. Performance parameters of all n-type OPAMP topology

Gain (V/V)	Gain (dB)	f_{3db} (Hz)	Unit gain freq. (Hz)	Phase margin (degrees)
19.8	25.9	188.8	1.6k	69

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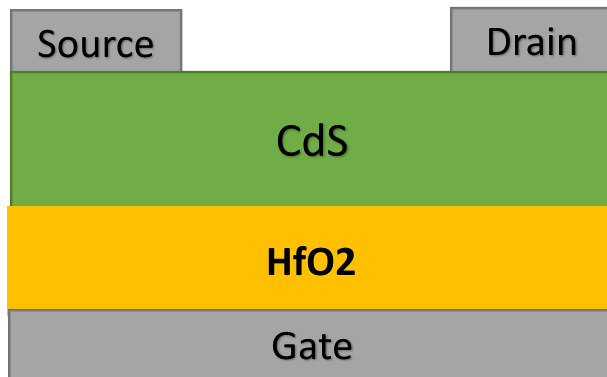
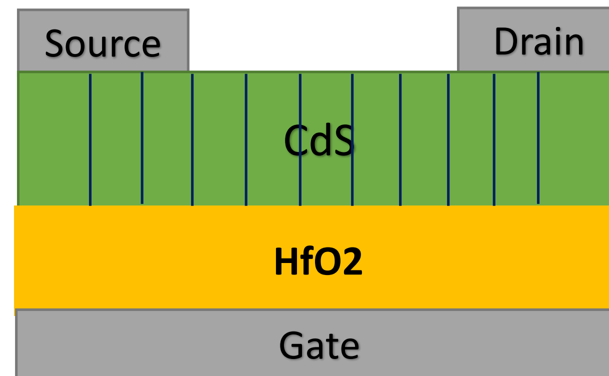
Device Simulation

Simulated device dimensions

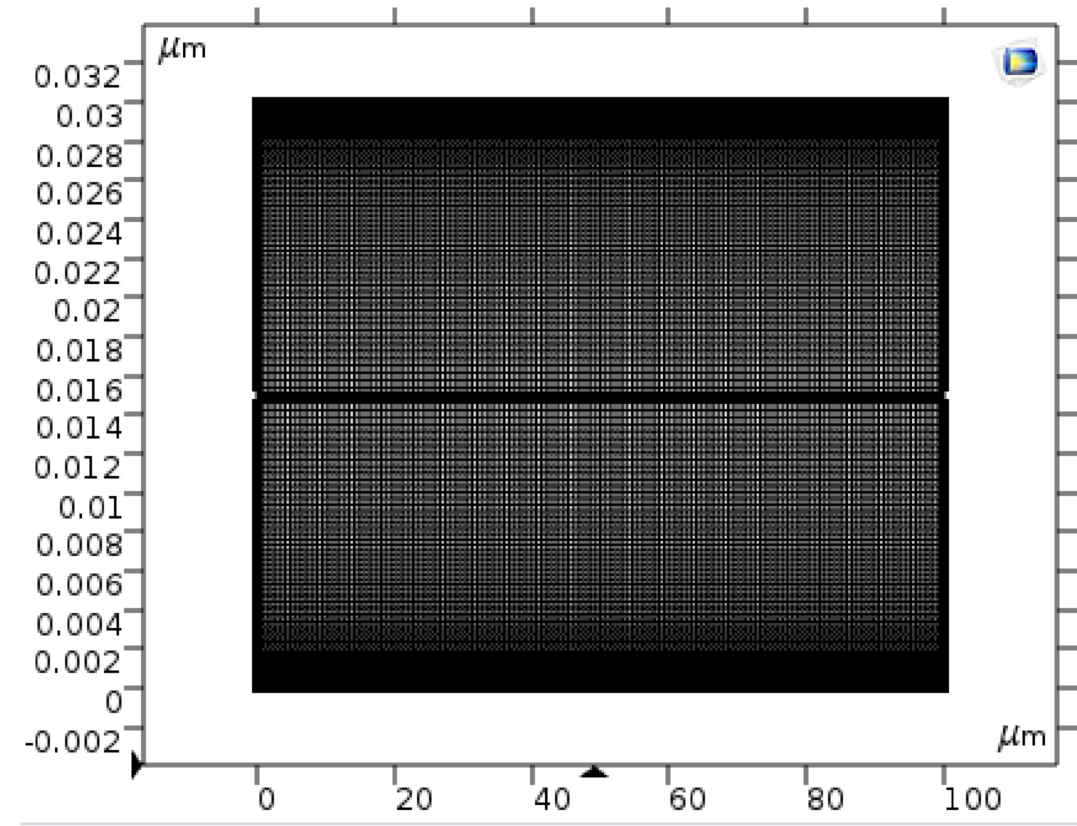
- 10 μm long gold S/D electrodes
- 100μm chromium gate electrode
- The gate oxide is a 90 nm thick HfO2.



(a)



(b)



(c)

Fig.5 (a) Uniform distribution of traps and defects, (b) Channel divided in to multiple grains, (c) COMSOL Mesh structure

Table 3 Summary of material parameters used in both simulation approaches

Material	Parameter	Values
CdS (active material)	Band-gap	2.42 eV
	Electron affinity	4.0 eV
	Electron low field mobility	4.3 cm^2/V-s
	Hole low field mobility	0.3 cm^2/V-s
	Thomas Claughey beta parameters	$\beta_p = 1$ $\beta_n = 2$
	Relative permittivity	8.9
	Donor doping	10^{16} cm^{-3}
	Density of states	10^{21} cm^{-3}
HfO_2 (dielectric)	Relative permittivity	17
CdS/HfO_2	Interface charge (number density)	10^{11} cm^{-2}
Al (S, D contacts) Cr (G contact)	Workfunction Work function	4.1 eV 4..37 eV

Computational Methods:
COMSOL **Semiconductor Module** is used to solve Poisson and Continuity equations:

$$-\nabla\cdot(\varepsilon\nabla V) = q(p - n + N_D^+ - N_A^-)$$

$$\frac{\partial n}{\partial t} = -\frac{1}{q}J_n - U_n$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}J_p - U_p$$

Exponential Trap distribution

$$g_{TA}(E) = n_{TA}\exp[\frac{E - E_C}{w_{TA}}]$$

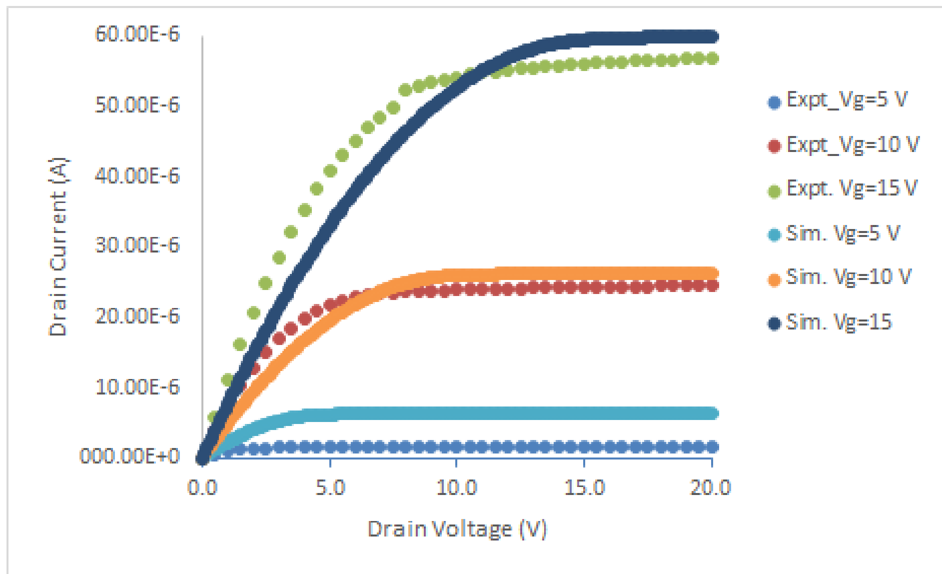
$$g_{TD}(E) = n_{TD}\exp[\frac{E_V - E}{w_{TD}}]$$

Gaussian Trap distribution

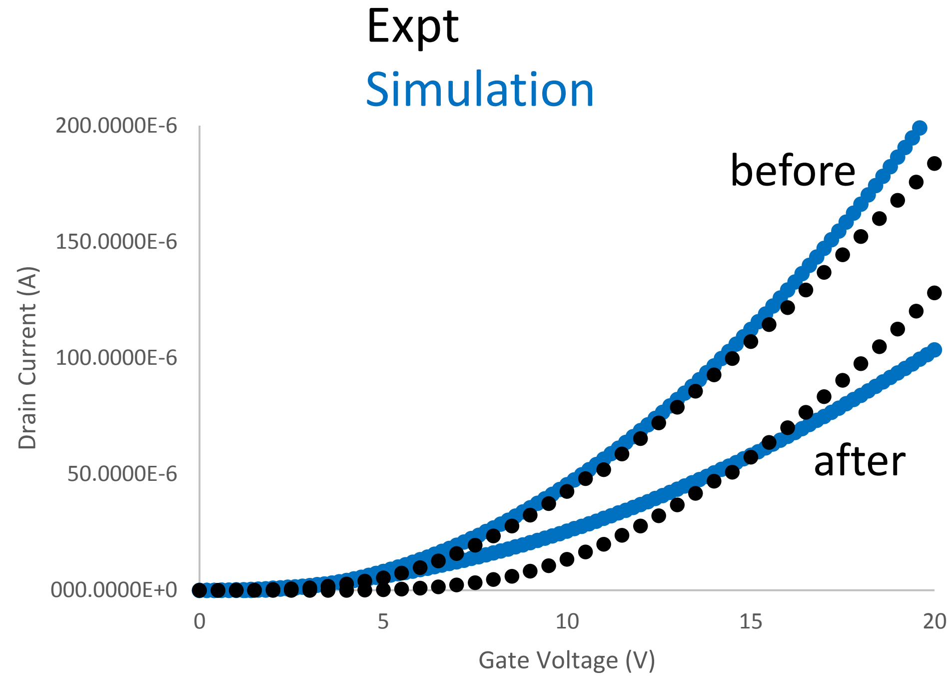
$$g_{GA}(E) = n_{GA}\exp\left[-\left(\frac{E_{GA} - E}{w_{GA}}\right)^2\right]$$

$$g_{GD}(E) = n_{GD}\exp\left[-\left(\frac{E - E_{GD}}{w_{GD}}\right)^2\right]$$

Results



(a)



(b)

Fig. 6. (a) Id – Vd curves for different gate voltage
(b) Id – Vg curves

Conclusion

- Semiconductor Module used to study threshold voltage shift
- Interface and bulk traps models used with Gaussian and exponential distribution
- Simulation issues - convergence